# Hybrid Voltage Balancing Control in 3-level Bridgeless Totem-pole PFC

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***Abstract* — Series connected Si MOSFETs provide a useful method to achieve greater voltage blocking capabilities in high-voltage power converter applications. However, the challenge imposed using this method is a naturally unbalanced voltage between series stacked devices. Voltage sharing imbalance can occur due to gate signal timing delay, device tolerances and layout parasitics potentially leading to overvoltage for a given device and subsequent converter failure. This article introduces a novel voltage balancing technique with additional transient voltage suppressor devices (TVS) to improve the reliability of 3-level bridgeless totem-pole (BTP) flying capacitor multilevel (FCML) converter comprised of low-voltage silicon based MOSFET devices. Relevant circuit diagrams and experimental results are both provided using a universal 9A-input current industrial PFC prototype converter.**

***Keywords* — *bridgeless totem-pole, PFC, hybrid voltage balance, flying capacitor, multilevel, voltage sharing.***

## I. Introduction

Since high-power rated MOSFET devices are higher in cost and are subject to greater on-resistance $R_{DS(ON)}$ with poor switching characteristics, a variety of topologies utilizing series stacked MOSFETs are used in order to reduce the cost and power losses in higher voltage applications [1], [2]. Several studies have been proposed regarding a voltage balancing control strategy for high voltage series-connected switching devices such as regenerative-snubber, active clamping and active gate driver [3], [4]. However, in case of a multilevel power conversion consisting of several series connected switching device pairs these approaches are not desired due to induced losses, greater complexity and high cost.

Moreover, hard switching is the most adopted technique in a variety of power converter applications. Hence, the only viable solution in reducing the switching loss is the lowering of a semiconductor device turn-on and turn-off times. However, this leads to higher dv/dt and di/dt of a switching device and a consequent EMI worsening, escalated device stress and the amplification of strain components. Based on these switching characteristic concerns, parasitic components as well as semiconductor physical constraints can no longer be ignored.

### A. *Characteristics of MOSFET devices*

Usually, practical power MOSFET devices are modeled with their terminal capacitances which are demonstrated in Fig. 1. The non-linearity induced by these voltage dependent parasitic terminal capacitances alongside the gate driver circuit output impedance dictates the switching performance. The variation in internal capacitances such as $C_{gs}$, $C_{gd}$ and $C_{ds}$ and their displacement currents (1),(2) and (3) during the turn-on transitions as well as other characteristic parameters are of great importance when series connected devices are driven in high power applications.

$$i_g = i_{gs} + i_{gd} \tag{1}$$

$$i_{gs} = C_{gs}\frac{dv_{gs}}{dt} \tag{2}$$

$$i_{gd} = C_{gd}\frac{dv_{gd}}{dt} \tag{3}$$

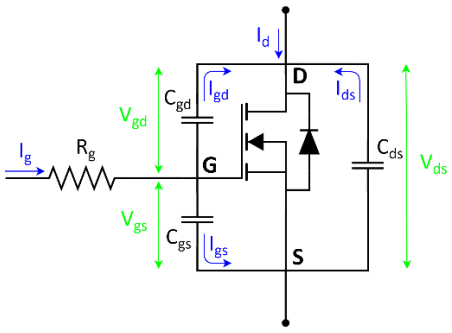


Fig. 1: Parasitic elements of a MOSFET device

### B. *Some title here*

The development of 3-level bridgeless totem-pole PFC utilizing series-connected 150V MOSFET switching devices has demonstrated that both low-cost and high efficiency (> 99%) can be achieved in CCM rectifier applications while offering additional advantages such as smaller magnetic components (4x reduction) and better EMI/EMC handling [5]. Nonetheless, to increase the reliability and compatibility with any MOSFET devices in the market there is an urge to develop a new voltage balancing technique for composite power switches that can address the inevitable variations of their characteristic parameters and other voltage distribution concerning aspects. Thereby, the main focus of this paper is to provide an extensive analysis of a hybrid flying capacitor voltage balancing control approach in 3-level bridgeless totem-pole PFC applications.

## II. 3-level Bridgeless Totem-pole PFC Topology

Power factor correction (PFC) converters are widely used in a variety of applications such medical, industrial, telecoms, etc. With higher energy consumption of these applications, the total amount of power loss is considerable. A conventional PFC converter containing the full rectifying diode bridge leads

to a larger conduction loss and imposes limits to the overall efficiency of a system. Thereby, considering a more efficient topology such as totem-pole bridgeless PFC is of great significance. Moreover, in contrast to other active PFC topologies, bridgeless totem-pole PFC is a preferred solution for its lowest component count and highest efficiency.

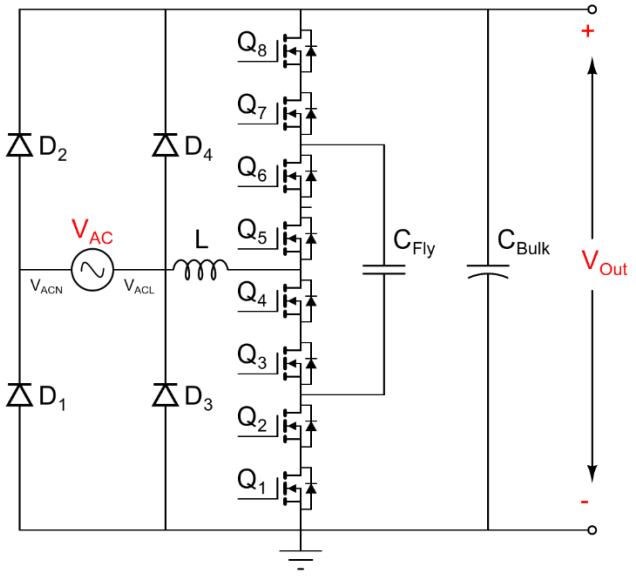


Fig. 2: 3-level bridgeless totem-pole PFC with inrush current diodes $D_{3\text{-}4}$

Fig. 2 demonstrates the simplified existing arrangement of a bridgeless totem-pole 3-level PFC converter. It consists of the following components:

- Single phase full-wave rectifiers $D_1$ and $D_2$ which conduct during the time close to $V_{AC} > 0V$ and $V_{AC} < 0V$, respectively.
- Inrush current handling diodes $D_3$ and $D_4$ which are only employed during startup and latch up modes of operation.
- Main PFC inductor denoted by L.
- High-frequency switching leg MOSFET transistors $Q_{1\text{-}8}$.
- An additional flying capacitor $C_{Fly}$ for voltage division and the output capacitor $C_{Bulk}$.

### A. *Phase Shift Modulation*

It is important to note that in HF switching leg each of the two series-connected 150V MOSFET devices such as $Q_1$ and $Q_2$ make up a composite device in which both are driven together. The 3-level MOSFET string is controlled using a phase-shift modulation (PSM) technique in which switches $Q_1$,$Q_2$ and $Q_7$,$Q_8$ make up a phase and are driven in complementary manner. The same applies to switches $Q_3$,$Q_4$ and $Q_5$,$Q_6$ forming another phase with an offset of 180°. The proposed modulation approach allows for the flying capacitor voltage to track the reference voltage of $V_{Out}/2$. Provided that the natural charge balance condition of the flying capacitor is met, each pair of the series connected MOSFETs are subject to a potential difference of around 200V. This is true for the converter nominal output voltage of 400V. Fig. 3 and Fig. 4 demonstrate PSM drive signals for bottom composite devices as well as the inductor current waveform during the time the control variable D < 0.5 and D > 0.5, respectively.

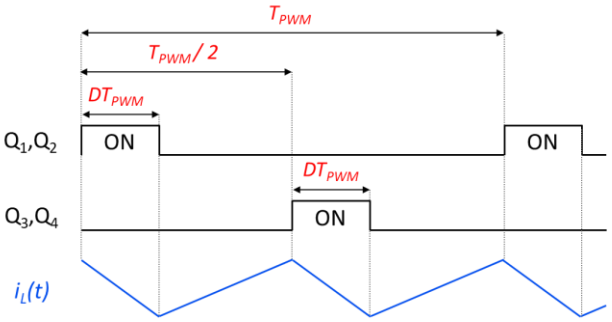


Fig. 3: PSM drive signals and inductor current (D < 0.5)

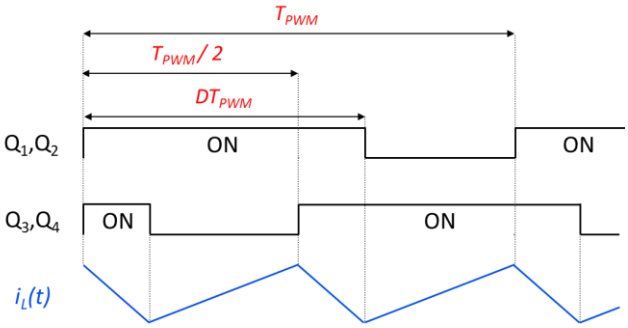


Fig. 4: PSM drive signals and inductor current (D > 0.5)

### B. *Converter model and control*

During the positive half-line cycle with an input voltage $V_{AC} > 0$, diode $D_1$ conducts connecting the neutral point ACN to local ground. Based on the state space averaging (SSA) method and other assumptions covered in [6], the control expression can be realised as follows:

$$L\frac{dI_L}{dt} = |V_{AC}| - D'V_{Bulk} \tag{4}$$

The differential equation (4) above implies that the inductor current $I_L$ can be programmed for a full duty ratio range of ($0 < D < 1$). In addition, the control variable D can be adjusted with response to different AC line $V_{AC}$, output voltage $V_{Bulk}$ or inductor current $I_L$ values.

During a negative half-line cycle with an input voltage $V_{AC} < 0$, diode $D_2$ is forward biased connecting the neutral point ACN to DC bus. Given the same SSA method and appropriate assumptions, the differential equation describing the model of the equivalent circuit during negative half-line cycle can be expressed as follows:

$$L\frac{dI_L}{dt} = |V_{AC}| + DV_{Bulk} \tag{5}$$

Similarly, based on the differential equation (5) above, the inductor current can be controlled and adjusted by manipulating the control variable D to account for changes in input voltage $V_{AC}$, inductor current $I_L$ and output voltage $V_{Bulk}$.

### C. *Flying Capacitor Active Balancing*

One of the attractive features of a multilevel flying capacitor converter is the natural voltage balance property. It allows for re-alignment of the flying capacitor voltage after some time during a steady-state operation without having to implement a new control strategy.

Based on (4) and (5), it is evident that inductor current $I_L$ and DC bus voltage $V_{Bulk}$ can be both regulated with reference to a variable duty ratio D. In principle, under natural balance conditions, the flying capacitor voltage $V_{FC}$ is supposed to follow the reference voltage of $V_{Bulk}/2$. However, the natural charge balance cannot be guaranteed under realistic transient or steady-state operating conditions. Consequently, an extended amount of switching cycles spent in an unbalanced condition, can lead to a voltage drift of the FC resulting in an increased voltage stress on switching devices and power loss. Likewise, in some applications the dynamics of natural charge balance could have a further adverse impact concerning the load and capacitance values.

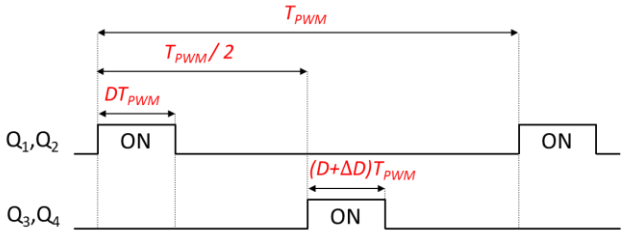


Fig. 5: Enhanced PSM with a duty cycle adjustment variable ΔD for effective flying capacitor voltage $V_{FC}$ balancing

Fig. 5 above demonstrates the active flying capacitor voltage balancing control mechanism for a three-level FC boost PFC. It is implemented as part of the enhanced PSM by utilising a technique of duty cycle adjustment to increase or decrease the charge/discharge time of the flying capacitor to enforce the balance. A separate control variable ΔD is chosen based on the required stabilization level. It is important to note that duty cycle adjustment variable can range anywhere from -D to D. However, only small values of ΔD (limited in software) are required to satisfy the natural balance requirements.

### *D. Gate Drive Technology*

The proprietary ICERGi gate drive technology allows for multilevel switching devices to be driven without a need for local power supply [7]. The isolated gate drivers enable precise channel matching allowing for minimal time offset in gate voltage of composite transistor devices. The operating principle of such gate driver is based on ferrite core magnetic coupling which allows for simultaneous transmission of both the drive signal and the adequate amount of power required to enhance the gate of the switching device. However, this technique alone cannot provide sufficient means of even voltage sharing between series connected devices, particularly when lower cost Si MOSFET devices are used such as 150V 35mΩ SQJ872EP with turn-on $t_{d(on)}$ – 9ns and slower turn-off $t_{d(off)}$ – 19ns delay as opposed to previously used 150V 16mΩ BSC160N15NS5 with $t_{d(on)}$ – 9.6ns and $t_{d(off)}$ – 10.8ns.

## III. Hybrid Voltage Balance Control in Flying Capacitors

Fig. 6 illustrates the proposed novel type of flying capacitor voltage balance control technique for the 3-level FC PFC converter. The arrangement is based on the 5-level FCML topology which ensures five distinct voltage levels [8]. The voltage balance enforcement circuitry consists of the additional flying capacitors $C_1$ and $C_3$ as well as the 6 x transient voltage suppressors denoted by $T_{1\text{-}6}$. However, unlike the 5-level FCML topology in which all flying capacitors are actively controlled using an appropriate PSM scheme, this approach employs actively controlled $C_2$ and passively controlled $C_1$ and $C_3$ with the help of voltage clamping TVS devices $T_{1\text{-}6}$, hence a hybrid voltage balance control. It is important to notice that due to the interconnection of additional flying capacitors in the circuit, each pair of devices is no longer a composite device. Instead, they should be treated as individual components.

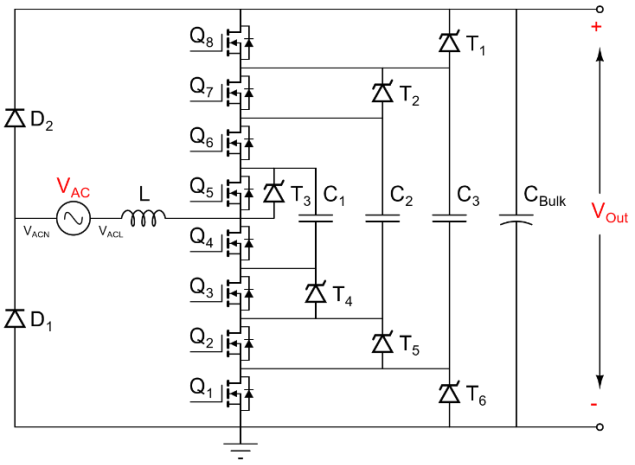


Fig. 6: Circuit diagram of a 3-level hybrid FC voltage balancing arrangement

Assuming that the nominal output bulk capacitor voltage is set to 400V, the insertion of both capacitors $C_1$ and $C_3$ allows for further operating voltage subdivision during the steady state operation of 100V and 300V, respectively. Voltage across the flying capacitor $C_3$ can be realized as the potential difference between the source of $Q_8$ and the drain of $Q_1$. Similarly, voltage across $C_1$ is given by the potential difference between the source of $Q_6$ and the drain of $Q_3$. Having said that, due to voltage distribution imbalance in concurrently driven devices, particularly during the heavy load conditions, the flying capacitor voltage can start to drift. Therefore, to provide a reliable passive flying capacitor voltage control, a total of 6 TVS devices are employed in the circuit. Two TVS devices are connected to each of the capacitors $C_1$ and $C_3$ as well as the additional $T_1$ and $T_5$ for a voltage initialization during power up condition of a PFC converter.

### *A. Component Selection*

Given the fact that during the steady state operation only a very small amount of current is flowing in and out of the additional flying capacitors, it allows for small ceramic capacitors of 47nF to be used. In addition, these capacitors are not required to store substantial amount of energy but must be large enough to remain stable between each switching cycle. A small standard form factor 0805 X5R ceramic capacitor with voltage rating up to 450V is sufficient for this purpose.

Voltage clamping components must be selected carefully so that the PFC converter operation does not undergo any adverse consequences during voltage initialization, startup or steady state operation (TABLE I). 100V 1SMBJ100D TVS devices are chosen to handle sudden or momentary overvoltage conditions for all FCs in the circuit. Some of the key component parameters that require consideration are listed below:

- Reverse stand-off voltage ($V_{RWM}$) parameter indicates the voltage level of each passively controlled flying capacitor without being significantly influenced by the TVS diode.

- Breakdown voltage ($V_{BR}$) denotes the voltage limit at which the TVS diode will begin conducting and consequently clamping the flying capacitor voltage. Both minimum and maximum values should be considered to ensure safe operating voltage range for each switching device.
- Maximum peak pulse power dissipation rating ($P_{PPM}$) indicates the instantaneous power dissipation level for a given pulse duration which is realised as a clamping voltage and peak pulse current product (6). It is an important measure while considering large voltage transient events such as input voltage surge.

$$P_{PP} = V_c * I_{PP} \tag{6}$$

TABLE I. COMPONENT PRIMARY CHARACTERSTICS

| ***Parameter*** | ***Description*** |
|---|---|
| **Transient voltage suppressor (TVS)** | |
| $V_{RWM}$ | 100 V |
| $V_{BR(min)}$ | 113 V |
| $V_{BR(max)}$ | 121 V |
| $P_{PPM}$ | 600 W |
| **Multilayer ceramic capacitor** | |
| Rated voltage (DC) | 450 V |
| Capacitance | 47 nF |
| Temperature characteristics | X5R |
| Code | 0805 |

### *B. Operating Principle of the Passive FC Voltage Control*

The working principle of this clamping arrangement is similar for both $C_1$ and $C_3$ and can be understood as follows. Suppose the output voltage $V_{OUT}$ is set to 400V, the actively controlled flying capacitor voltage $V_{C2}$ is tracking $V_{OUT}/2$ (200V) and the avalanche breakdown voltage of TVS devices are said to be 113V. As a result, during the time both $Q_7$, $Q_8$ are turned ON and $Q_1$, $Q_2$ are turned OFF, the upper voltage clamping limit for 300V flying capacitor is given by $V_{C3(max)} = V_{C2} + V_{T2}$. When $Q_7$, $Q_8$ are turned OFF and $Q_1$, $Q_2$ are turned ON the lower camping limit corresponds to $V_{C3(min)} = V_{Bulk} - V_{T6}$ which yields that all individual outer switching devices $Q_1$, $Q_2$ as well as $Q_7$ and $Q_8$ are not subject to greater voltages than the rated maximum breakdown voltage of the TVS device of ±20V from the intended voltage level of 100V.

Similarly, the inner switching leg device $Q_{3\text{-}6}$ voltage levels are dictated by the flying capacitor $C_1$ with the help of $T_3$ and $T_4$. Considering the time when the pair of devices $Q_5$, $Q_6$ are switched ON, the upper voltage clamping limit of $C_1$ can be expressed as $V_{C1(max)} = V_{T3}$. In the opposite case when the upper pair of devices $Q_3$, $Q_4$ are turned ON and $Q_5$, $Q_6$ are turned OFF, the lower voltage threshold is given by $V_{C1(min)} = V_{C2} - V_{T4}$. Given the above expressions for both flying capacitors $C_1$ and $C_3$ the maximum voltage fluctuation range for each can be summarized in the following equations (7) and (8), respectively.

$$V_{C2} - V_{T4} \leq V_{C1} \leq V_{T3} \tag{7}$$

$$V_{Bulk} - V_{T6} \leq V_{C3} \leq V_{C2} + V_{T2} \tag{8}$$

### *C. FC voltage initialization*

FC multilevel converters are required to achieve and maintain the voltage balance of all flying capacitors during transient and steady state operations. Having said that, during the power up of the PFC converter, all of the flying capacitors are expected to be discharged with almost no potential difference between their terminals. Once the high DC voltage is applied to DC bus, MOSFET devices could undergo severe voltage overstress potentially leading to the overall system failure. To avoid this issue an additional pair of TVS devices $T_1$ and $T_2$ are added to the circuit. This is imperative in order to ensure that all FCs are pre-charged to the minimum required voltage level before start-up condition. It is worth noting that the pre-charge voltage level for each capacitor is dictated by the breakdown voltage ($V_{BR}$) of TVS devices as well as the magnitude of the rectified AC input voltage ($V_{Bulk}$). To slow down the precharge rate for all FCs and the bulk capacitor is achieved by placing a negative temperature coefficient (NTC) thermistor on the input side of the PFC converter.

## IV. SIMULATION IMPLEMENTATION AND RESULTS

For the purpose of a better understanding of the circuit operation and improved design efficiency, the simulation model is implemented in LTspice software (Fig. 7). The main purpose of the preliminary PFC simulation model is to observe the voltage initialization of all flying capacitors before the startup.

### *A. Simulation Parameters*

The component values are chosen to be as close to the practical implementation as possible. Both capacitors and inductors in the circuit are given zero initial conditions. The input signal to the system is selected to be $230V_{AC}$ followed by two-stage mains input filter. The inrush current is addressed by placing a 10Ω NTC thermistor before the line rectification diodes $D_{9\text{-}12}$. It is important to note that the parasitic elements are not considered in detail for the purpose of this simulation behavior. Taking this into account, the main PFC inductor (500µH) as well as all of the capacitors are only modeled with a small series resistance (ESR) of 100µΩ. The switching leg devices $Q_{1\text{-}8}$ are modeled with body diodes and are defined to stay in a blocking state. The output of the system is arranged by a 500µF bulk capacitor placed in parallel with a resistor limiting the output power to 10W after the initial precharge routine. Finally, the simulation model for TVS devices is specified with $V_{BR}$ of 113V. The lower blocking voltage level is selected due to the minor power dissipation requirement during power up. In addition, the datasheet of the corresponding TVS device used in a hardware prototype specifies a very tight $V_{BR}$ tolerance of ±3.5%.

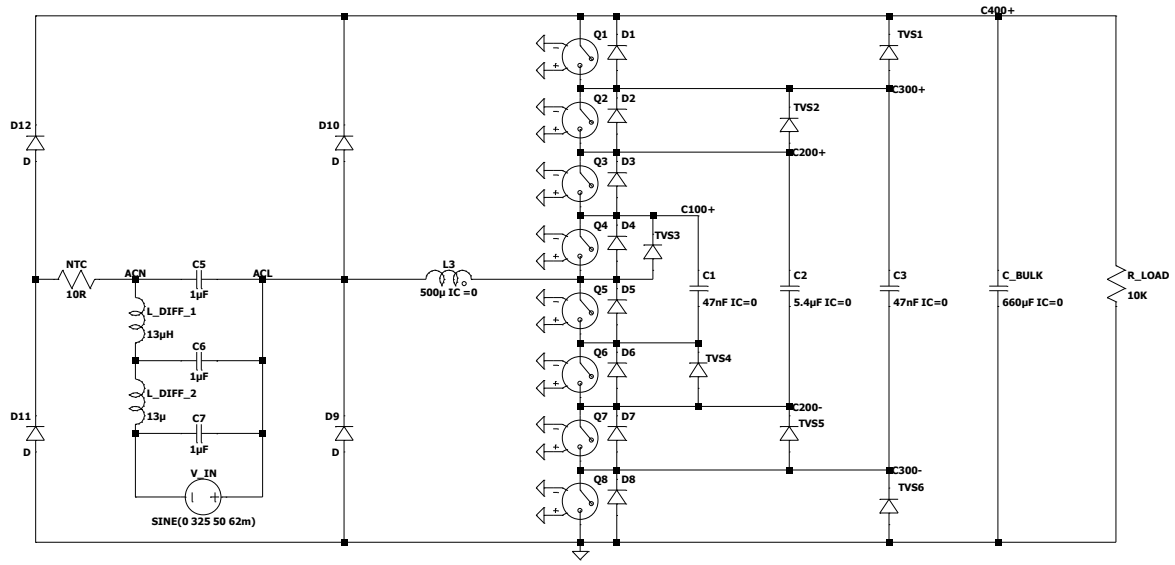


Fig. 7: LTspice simulation model of the 3-level BTP PFC

### B. *Simulation Results*

The simulation results are presented in Fig. 8. It is clear that the precharge sequence commences first with the energy transfer to the bulk capacitor $C_{Bulk}$. As soon as the output voltage exceeds the breakdown voltage of the outer TVS devices it will begin to conduct allowing for $C_3$ to be charged up. In this case, $TVS_1$ or $TVS_6$ will be conducting based on the polarity of the AC line voltage. Similarly, when the output voltage approaches 200V, $C_2$ will start to slowly charge up with the help of $TVS_2$, $TVS_5$ as well as $TVS_1$ and $TVS_6$. Finally, in accordance with the simulation results the same holds true for the flying capacitor $C_1$ which gets energized with the use of $TVS_4$. One can observe that after voltage initialization none of the switching devices are subjected to greater blocking voltages than the specified TVS $V_{BR}$ of 113V. Maximum instantaneous power dissipation of any four-given outer TVS devices are found to be no greater than 8W with a total current pulse duration up to 4ms.

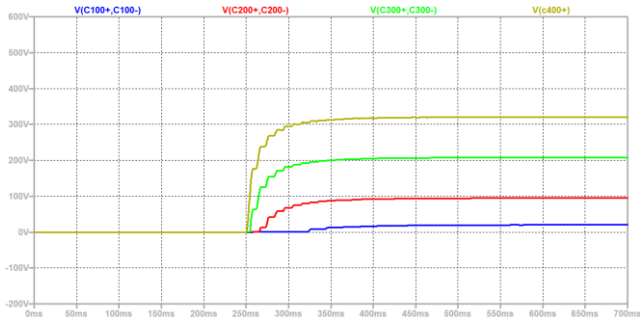


Fig. 8: Simulation results of voltage initialization (BLUE – $C_1$, RED – $C_2$, GREEN – $C_3$, YELLOW – $C_{Bulk}$)

## V. Experimental Validation

### A. *Hardware Prototype*

To validate the design of the proposed hybrid voltage balancing technique in hardware, 4-layer PCB was developed accommodating 8 x 150V SQJ872EP MOSFETs, 6 x SMBJ100D TVS devices as well as the flying capacitors $C_1$ and $C_3$ of 47nF and $C_2$ with the total capacitance of 5.4µF (Fig. 9). In addition, Fig. 10 below demonstrates the corresponding PCB layout of the power board design.

Fig. 9: Power board prototype used in a 2 kW PFC

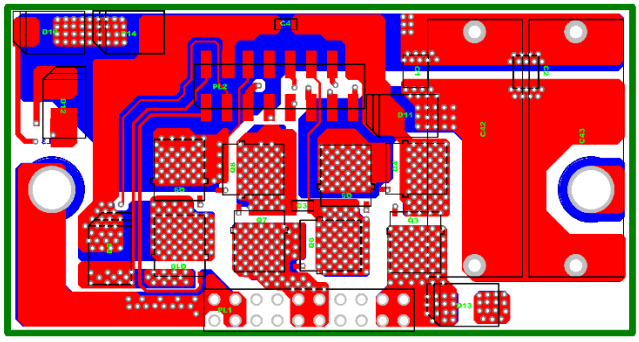

Fig. 10: 2-layer PCB layout of the power board design

In order to capture waveforms of interest, the universal 9A-input (2kW) PFC prototype is utilised including both control drive and power boards as seen in Fig. 11. The converter is designed to be operating with a switching frequency of 66kHz and the nominal output voltage of $400V_{DC}$. Moreover, the system is capable to operate with the universal line voltage in the range of $85V_{AC}$ – $265V_{AC}$ as well as the maximum output power rated at 1kW with $115V_{AC}$ and 2kW with $230V_{AC}$.

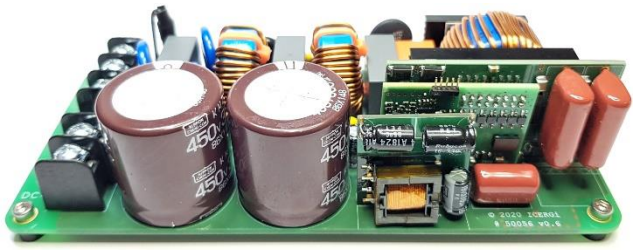

Fig. 11: Compact 75W/in$^3$ 2kW PFC hardware prototype (158mm x 72mm x 38mm)

### B. *Voltage Initialization*

The experimental waveforms during FC voltage initialization are captured with the input voltage of $230V_{AC}$ and the output power level of 10W. The resultant waveforms are presented in Fig. 12 below. Note that in this case the PFC converter is still not switching with all MOSFET devices remaining in a blocking state thereby no boosting of the output voltage is performed.

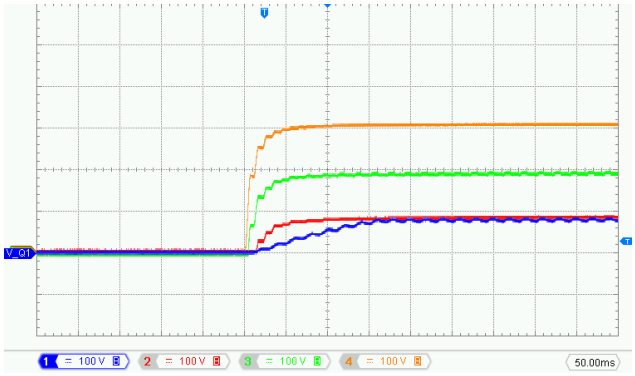

Fig. 12: Experimental voltage initialization waveforms of a hybrid voltage balancing in flying capacitors (BLUE – $C_1$, RED – $C_2$, GREEN – $C_3$, YELLOW – $C_{Bulk}$)

Once the FC voltage precharge transient is completed, all of the flying capacitors are initialized close to the expected simulated voltage levels. It should be noted that the differential signal waveform of $C_1$ on the oscilloscope is not correct. This was confirmed with the use of high-precision DMM. The comparison of the simulated and experimental results is provided in TABLE II below.

TABLE II. SIMULATED VS EXPERIMENTAL VOLTAGE INITIALIZATION RESULTS

| ***Results*** | $V_{C(1)}$ | $V_{C(2)}$ | $V_{C(3)}$ | $V_{C(Bulk)}$ |
|---|---|---|---|---|
| Simulated | 21V | 95V | 208V | 320V |
| Experimental | 18V | 91V | 200V | 320V |

### C. *Start-up*

Fig. 13 demonstrates capacitor voltage waveforms during the PFC converter start-up. Inductor current is programmed to follow the AC line voltage while boosting the output voltage to the specified nominal voltage of 400V. The performance of the proposed hybrid voltage balancing arrangement is observed to be stable. All three FCs are further energized at a similar rate allowing for even voltage distribution across all four levels. To verify the performance of the circuit, PFC start-up was tested at different output load and input voltage conditions.

Fig. 13: Experimental start-up waveforms (BLUE – $C_1$, RED – $C_2$, GREEN – $C_3$, YELLOW – $C_{Bulk}$)

### D. *Steady-state Operation*

To analyse the steady state performance of the proposed hybrid voltage balancing control in flying capacitors, the system is supplied with the input voltage of $115V_{AC}$. The nominal output voltage level is set to be 400V with a resistive output load of 1kW. Fig. 14 indicates that both flying capacitor $C_1$ and $C_3$ voltage levels for each half line cycle are under the specified TVS maximum breakdown voltage $V_{BR(max)}$ of around 120V.

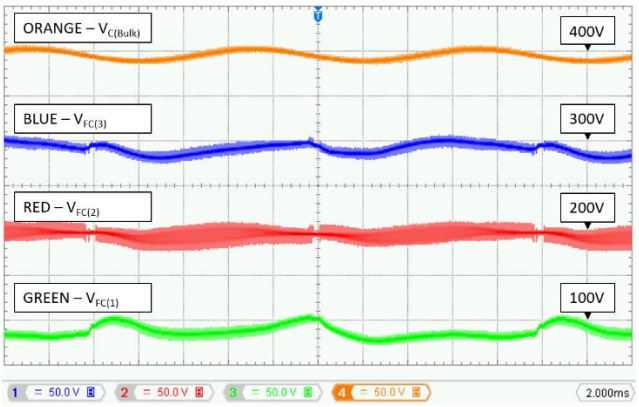


Fig. 14: Experimental steady state waveforms of a hybrid voltage balancing in flying capacitors

Furthermore, to gain more insight into the effectiveness of the new FC voltage balancing method, switching waveforms of two bottom MOSFET devices $Q_1$ and $Q_2$ are demonstrated in Fig. 15 below. It should be noted that during this test the PFC power board contains neither TVS nor the additional ceramic capacitor devices as demonstrated in Fig. 2. The left side of the image illustrates a voltage distribution between hard-switched MOSFET devices during a positive half line cycle. Evidently, voltage imbalance problem becomes more pronounced with higher instantaneous AC peak current to the system. Voltage disparity of two series connected MOSFETs is measured to be around 50V. More importantly, $Q_1$ device undergoes a turn-off blocking voltage of around 130V followed by an even larger dv/dt transient close to 150V.

Fig. 16 indicates the improved voltage equalization using the proposed hybrid voltage balancing technique. Recall that in this arrangement each of the MOSFETs in the string are treated as a separate device. As expected, the voltage imbalance between bottom two devices $Q_1$ and $Q_2$ is reduced. This also holds true for the remaining transistors in the switching leg.

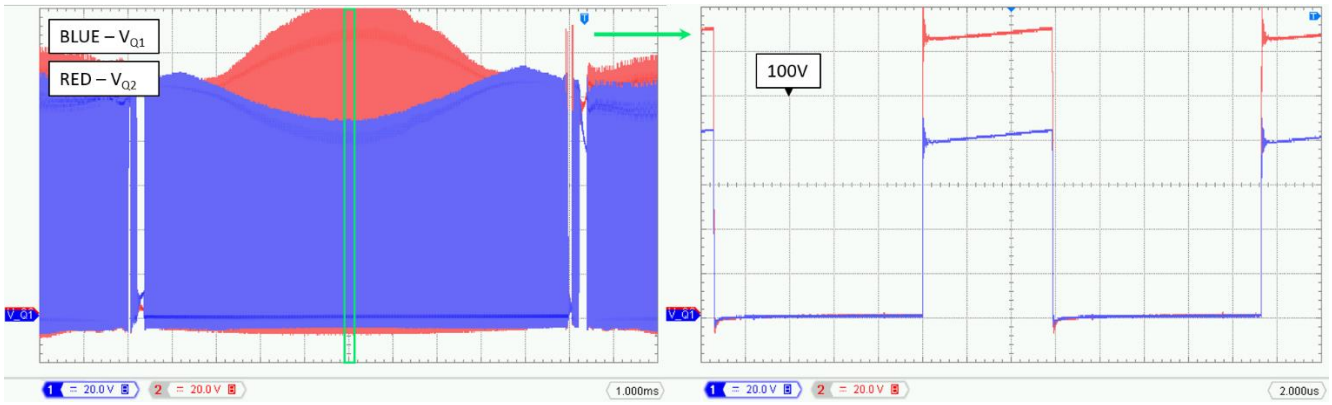

Fig. 15: Switching waveforms of $Q_1$ and $Q_2$ without passive voltage balancing circuit

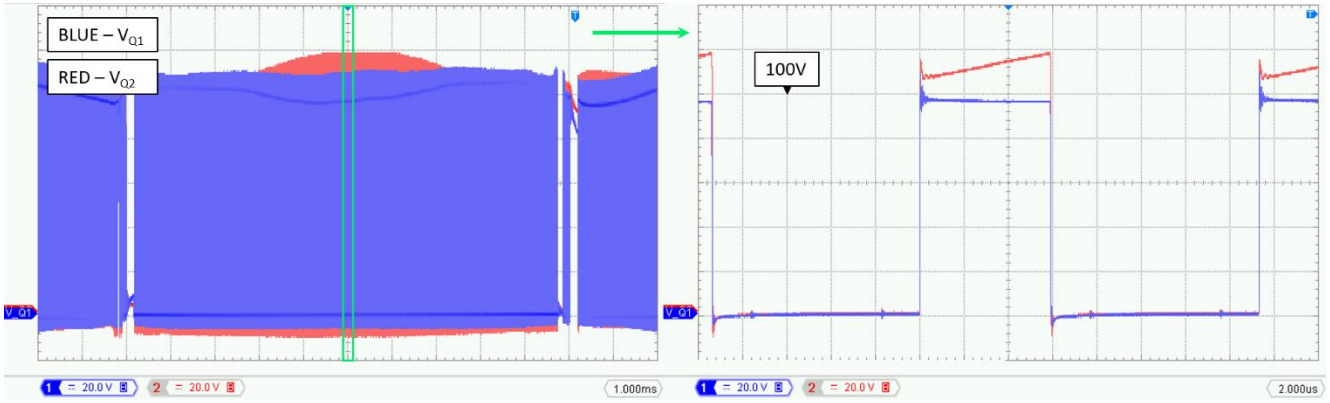

Fig. 16: Switching waveforms of $Q_1$ and $Q_2$ with passive voltage balancing circuit

### *E. Power Loss*

The power loss estimation is carried out using the PFC converter operating at line voltage of $115V_{AC}$ with and without the additional passive voltage control circuit. Test results provided in Fig. 17 indicate the additional power loss in the system under steady state operation at different output load levels.

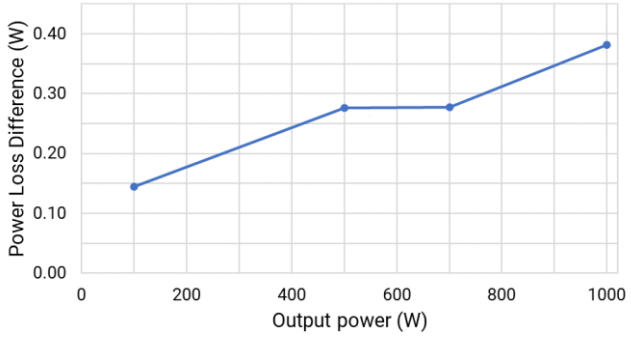

Fig. 17: Additional power loss due to hybrid voltage balancing control

### *F. PFC Converter Performance*

Fig. 18 and Fig. 19 present the efficiency and the total power loss of the 9A-input universal (2kW) PFC converter, respectively. The performance data is captured with the PFC output voltage set to 400V and the adequate forced air cooling to deliver the rated power. The efficiency data accounts for the losses in EMI filter, 12V bias supply as well the additional circuitry of the hybrid voltage balancing arrangement.

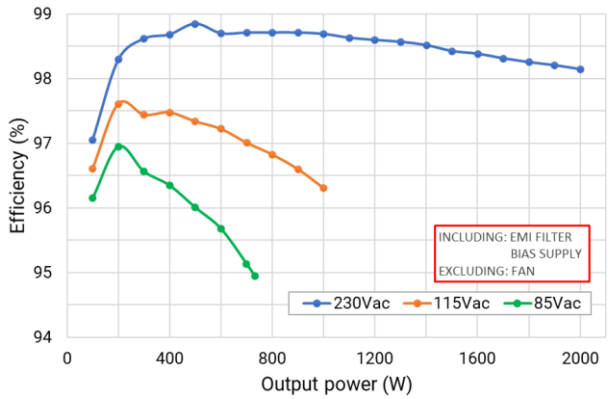

Fig. 18: 9A-input universal PFC efficiency

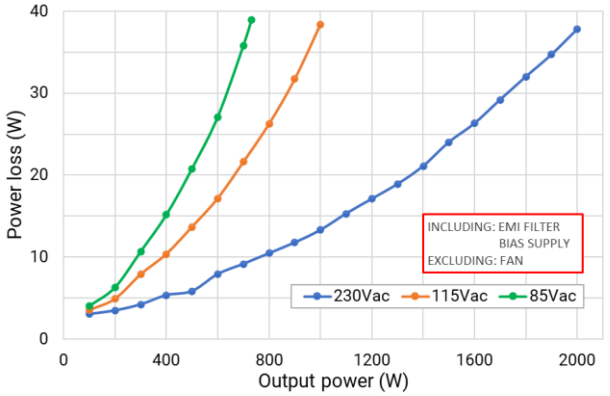

Fig. 19: 9A-input universal PFC total power loss

## VI. Conclusion

This study introduces the need for a voltage balancing control for series connected MOSFETs due to their inevitable difference of timing delays and other characteristic parameters. The proposed novel flying capacitor hybrid balancing method based on actively controlled $C_2$ in conjunction with passively controlled $C_1$ and $C_3$ is demonstrated. To mitigate voltage unbalance during turn-off operations, a simple circuit consisting of only passive components is added to the existing 3-level PFC converter. As opposed to more complex voltage balancing arrangements, the proposed method benefits from low cost and great reliability.

Some of the technology aspects as well as the implementation details covered in this paper may be subject of patent applications.

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